UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,235	03/26/2004	James N. Dieffenderfer	20421-00072-US	9456

48019 7590 03/28/2007

CONNOLLY BOVE LODGE & HUTZ LLP
(FOR IBM RALEIGH)
P.O. BOX 2207
WILMINGTON, DE 19899-2207

EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,235	DIEFFENDERFER ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-14* is/are allowed.

6)☒ Claim(s) *1-11 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been considered. Claims 1-4, 6-10, and 12-15 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 04 January 2007.

Allowable Subject Matter

3. Claims 12-14 are allowed.

4. The following is an examiner's statement of reasons for allowance: Independent claim 12 recites the limitations "wherein, depending on a value of the valid bit, said multiplexer supplies said one of the plurality of locations in the instruction queue with either an output of one of the decode stages or an output of the instruction cache, wherein, when the output of the instruction cache is supplied to said one of the plurality of locations in the instruction queue, the output of the instruction cache is simultaneously supplied to said one of the decode stages." In essence, this limitation states that, depending on a valid bit, the instruction queue and the decoder are loaded with the same instruction from the instruction cache at the same point in time. This was not found in the prior art. The prior art found has taught the same instruction can be found in the instruction queue or the decoder at different points in time and that the instruction queue and the decoder load different instructions from the instruction cache at the same time, but not the same instruction at the same time.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification has not adequately enabled one of ordinary skill in the art to implement the limitations of claim 15. The claim states that the processing stages execute instructions from, presumably, the instruction queue. However, some of the instructions in the queue are not decoded, since they were loaded directly into the instruction queue due to invalid data being in the queue. This means that some of the instructions in the instruction queue are un-decoded instructions, and, if the instruction were executed at that point, it would be executed incorrectly. The Examiner could not locate any point in the specification where the inventors described how an un-decoded instruction would be executed correctly in the execution pipeline. Therefore, this limitation has not been enabled adequately for a person of ordinary skill in the art to build without undue experimentation.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-8 and 10-14 are rejected under 35 U.S.C. 102(b) as being taught by Joshi et al., U.S. Patent Number 5,954,815 (herein referred to as Joshi).

10. Regarding claim 1, Joshi has taught a method for decreasing the latency between an instruction cache and a pipeline processor having a plurality of parallel execution stages, each execution stage having a decode stage and an instruction queue for sequentially processing instructions being processed by said processor, comprising:

a. Determining whether said decode stage and said instruction queue do not have valid data (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7); and

b. Simultaneously inserting instructions from said instruction cache in parallel to said decode stage and said instruction queue when said decode stage and instruction queue contain invalid data (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

11. Regarding claim 2, Joshi has taught the method of claim 1 further comprising:

a. Processing said cache instructions from said cache sequentially through said decode stage and said instruction queue when valid data exists in said instruction queue (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line

34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

12. Regarding claim 3, Joshi has taught a method for processing instructions in a pipelined processor having a series of pipelined stages which reduces latency between an instruction queue and a pipeline processor, the method comprising:

a. Serially fetching a plurality of instructions to be executed in said pipeline processor from a cache memory (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

b. Decoding each of said fetched plurality of instructions in a first stage of said pipeline processor to determine if an execution branch is to be taken (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

c. Simultaneously loading one or more of said fetched plurality of instructions into said instruction queue and into said decoder when said instruction queue and decoder are empty (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

d. Sequentially loading each of said fetched instructions into said instruction queue from said decoder when said instruction queue and said decoder are not empty (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34;

column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7); and

e. Shifting contents of said instruction queue to produce an instruction from said instruction queue for processing in subsequent pipeline stages (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

13. Regarding claim 4, Joshi has taught the method of claim 3 wherein said decoder identifies each of said plurality of fetched instructions loaded in said queue at the same time as said instructions which are loaded in said decoder as valid or invalid during a subsequent cycle of said pipeline processor if an execution branch is not taken (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

14. Regarding claim 5, Joshi has taught the method for processing instructions in a pipelined processor according to claim 3 wherein said instruction queue contents are shifted left to an output port connected to plural pipelined processor stages (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7). In regards to Joshi, the contents of the queue are shifted from ibuf0 to ibuf1 to ibuf2, etc., as shown in Figure 3. The shift is relative to the position of the buffer, so it could be left or right. It does not matter, the operation would remain the same.

15. Regarding claim 6, Joshi has taught a method for executing instructions in a pipelined processor comprising: sequentially fetching the addresses of instructions to be executed by said pipelined, the method processor;

a. Sequentially fetching instructions to be executed by said pipelined processor (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

b. Determining if said fetched instructions are stored in a cache memory (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

c. Determining whether both a decode stage of a decoder and an instruction queue stage of an instruction queue of said pipelined processor are empty (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

d. Simultaneously loading said fetched instructions from said cache memory into said decode stage and into said instruction queue stage in parallel when both said decode stage and said instruction queue stage are empty (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7); and

e. Sequentially reading out said instruction queue instructions for execution in said pipelined processor (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

16. Regarding claim 7, Joshi has taught the method of claim 6, further comprising:

a. Loading only said decode stage with said instructions when said instruction queue stage contains valid data, and sequentially transferring said instructions to said instruction queue when a position in said instruction queue is available (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

17. Regarding claim 8, Joshi has taught the method of claim 7, further comprising

a. Identifying one of said fetched instructions as a branch instruction if said decoder predicts that a branch is being taken (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7); and

b. Inhibiting transfer of subsequent instructions from said decoder to said instruction queue (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7). In regards to Joshi, instructions are fetched from the predicted target, so the subsequent instructions directly following the branch are not fetched, i.e. inhibited from transfer to the decoder.

18. Regarding claim 10, Joshi has taught the method of claim 6, further comprising:

a. Determining a state of a valid bit in a location in said instruction queue so as to determine whether said location contains valid data (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

19. Regarding claim 11, Joshi has taught the method for executing instructions in a pipeline processor according to claim 7, wherein said instructions are transferred from said decode stage to said instruction queue each time an instruction is read from said instruction queue (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al., U.S. Patent Number 5,954,815 (herein referred to as Joshi), as applied to claim 7 above, in view of Free On-Line Dictionary of Computer (herein referred to as FOLDOC). Joshi has taught the method of claim 7, further comprising forwarding said fetched instruction to said decode stage for sequential transfer to said instruction queue (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column

7, line 33; Figure 2A; Figure 3; and Figure 7). Joshi has not taught fetching an instruction from a main memory when said branch instruction is not in said cache memory. FOLDOC has taught an instruction from a main memory when said instruction is not in said cache memory (FOLDOC term "cache miss" ©1997). Joshi has taught that the instructions are fetched from the instruction cache (Joshi column 4, lines 1-4 and Figure 3), but has not taught where the instruction is fetched from when the cache does not contain the instruction. FOLDOC has taught that, when there is a cache miss, i.e. data cannot be found in a cache, the data is fetched from main memory (FOLD term "cache miss" ©1997). A person of ordinary skill in the art at the time the invention was made would have recognized that fetching data from main memory when it is not in the cache is necessary for execution to proceed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the cache miss of FOLDOC in the device of Joshi to ensure execution continues.

Response to Arguments

22. Applicant's arguments filed 04 January 2007 with regards to claims 1-11 have been fully considered but they are not persuasive. Applicants argues in essence on pages 7-10 "...Applicants' disclosed and claimed invention simultaneously loads the same instructions into both the decoder stage and the instruction queue when they are empty or contain invalid data..." This has not been found persuasive. Taking claim 1 as exemplary, the claims recite "simultaneously inserting instructions from the instruction cache in parallel to said decode stage and instruction queue when said decode stage and said instruction queue contain invalid data." There is no language in the claims recited with regard to the same instruction being inserted simultaneously into the instruction queue and the instruction decoder. Only that instructions

from the instruction cache are inserted simultaneously. The instructions being loaded into the instruction decoder and instruction queue are all from the instruction cache. The instructions in the decoder enter into the instruction queue after the decoder is done, when there is space in the instruction queue, e.g. invalid data in the queue. After the instruction leaves the decoder and enters the instruction queue, the decoder no longer has any valid data and another instruction from the cache can be loaded. Hence, the decoder and instruction queue are inserting instructions that are from the instruction cache simultaneously, but they are not the same instructions. However, the instructions being inserted do not need to be the same according to the claim language, they just need to originate from the instruction cache, which all instruction being inserted are.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
19 March 2007

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100